The GigaFitter for Fast Track Fitting based on FPGA DSP Arrays

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For the SVT Collaboration
SVT: A Success for CDF

- SVT provides offline quality 2D tracking at Level 2 Trigger of CDF combining silicon detector and drift chamber information.

- It allows to implement selections on the impact parameter of the tracks at trigger level to look for long living particles: b-quark, c-quark enriched samples without lepton requirements! (first time at hadron colliders)

- Thanks to SVT:

  - $B \rightarrow hh$
  - $B_s$ Mixing

On-line Plot!
On-Line Tracking: the SVT way

A two steps Algorithm

1. Find low resolution track candidates called "roads". Solve most of the pattern recognition.

2. Then fit tracks inside roads. Thanks to 1st step it is much easier.

Pattern Recognition (AM)

Track Fitting (TF)
Track Fitter Algorithm

- Linear expansion in the hit positions $x_i$ reduces track fitting to scalar products:

\[ p_i = \vec{f}_i \cdot \vec{x} + q_i \]

- $p_i$: track parameters ($P_t, \phi_0$ and Impact Par.)
- $\vec{f}_i, q_i$: know constants.
- $\vec{x}$: vector of hit positions

- hit → 18 bits.
- Old FPGA → at maximum 8x8 multipliers. → Large Memory corrections
- Scalar products splitted in two terms:

**Pre-calculated term:**
One for each Road

**On-line evaluated with 8x8 bit multipliers**
The GigaFitter core

• Technology improves, of course…
• Today new FPGAs equipped with many 25x18 bit multipliers are available, like the:

Xilinx VIRTEX 5: 65 nm- 550 MHz devices
XC5VSX95T: 160 x 46 CLB Array (Row x Col)

244 39kbits BlockRams or Fifos + 640 DSP Slices (organized in columns)

It allows to come back to the original scalar product with the full hit positions using 18x18 bit multipliers

\[ p_i = \vec{f}_i \cdot \vec{x} + q_i \]

No need for pre-calculated terms (stored in big memories)
DSP Slices

DSP: dedicated arithmetic logic

CLB: “And”, FF, and look-up tables
The CDF Silicon Vertex (SVX) is organized in 12 phi wedges. For each wedge, a TF (implemented in a Pulsar board) is coupled to the corresponding AM. The CDF Trigger/DAQ uses a Pulsar board (general purpose board) with pre-calculated terms for track fitting. There are 12 Pulsars, one for each TF.
The Full New System for SVT

4 wedge connectors on each mezzanine → possible up to 6x4=24 fits in parallel

3 mezzanines = 12 wedges
4th mezzanine → large memory for non-linearity corrections

Pulsar Board
Advantages

- **Shorter processing Time**

- **Deleted one location per pattern memories → Associative Memories potentially unlimited, many more Patterns for:**
  - High Pt Physics: enlarge lepton acceptance
  - B Physics: improve track $P_t$ and Impact Parameter acceptance

- **Many constant sets: improve tracking efficiency.**

- **Simultaneous fits of different layer configurations: improve efficiency.**

- **Very compact system. (1 board instead of 12 !)**
Conclusions

• The GigaFitter is an upgraded Track Fitter, based on new generation FPGA DSP arrays.

• An important step forward for dedicated powerful processors for on-line track reconstruction at hadron colliders, following the strategy successfully implemented by the SVT at CDF.

• The GigaFitter is expected to upgrade the SVT system in the last data taking period of the CDF experiment, BUT...

• ... the GigaFitter is in general a very powerful processor to be used wherever many scalar products at high working frequency are needed.
BACKUP
The GigaFitter

6 input LUT Inside Slices

6x6x5 + 7x7 = 229 DSP slices

4/5 silicon 5/5 silicon

Choose the best chi**2

Choose best chi**2

SVT FiFo 35 MHz

II FiFo 70 MHz

Block RAMs

Lay0-Ram or SR

Lay1- Ram or SR

Lay2- Ram or SR

Lay3- Ram or SR

Lay4-Ram or SR

XFT-Ram or SR

Comb - FiFo

7 Mult+7 Σ

6 Mult+6 Σ

6 Mult+6 Σ

6 Mult+6 Σ

6 Mult+6 Σ

6 Mult+6 Σ

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