Quantum Technology Experimental Platform (Quantep) project

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Photonic Integrated Circuit

- PICs, or optical chips, integrate multiple photonic functions for information signals imposed on optical wavelengths.
- Advantages:
- Small stochastic noise level.
- PICs are strongly pursued for classical computing purposes, and the core components necessary are under research. PICs are not only CMOS compatible but also can be built with nothing changed in CMOS fabrication techniques and standards.

Silicon photonics with Silicon-On-Insulator technology

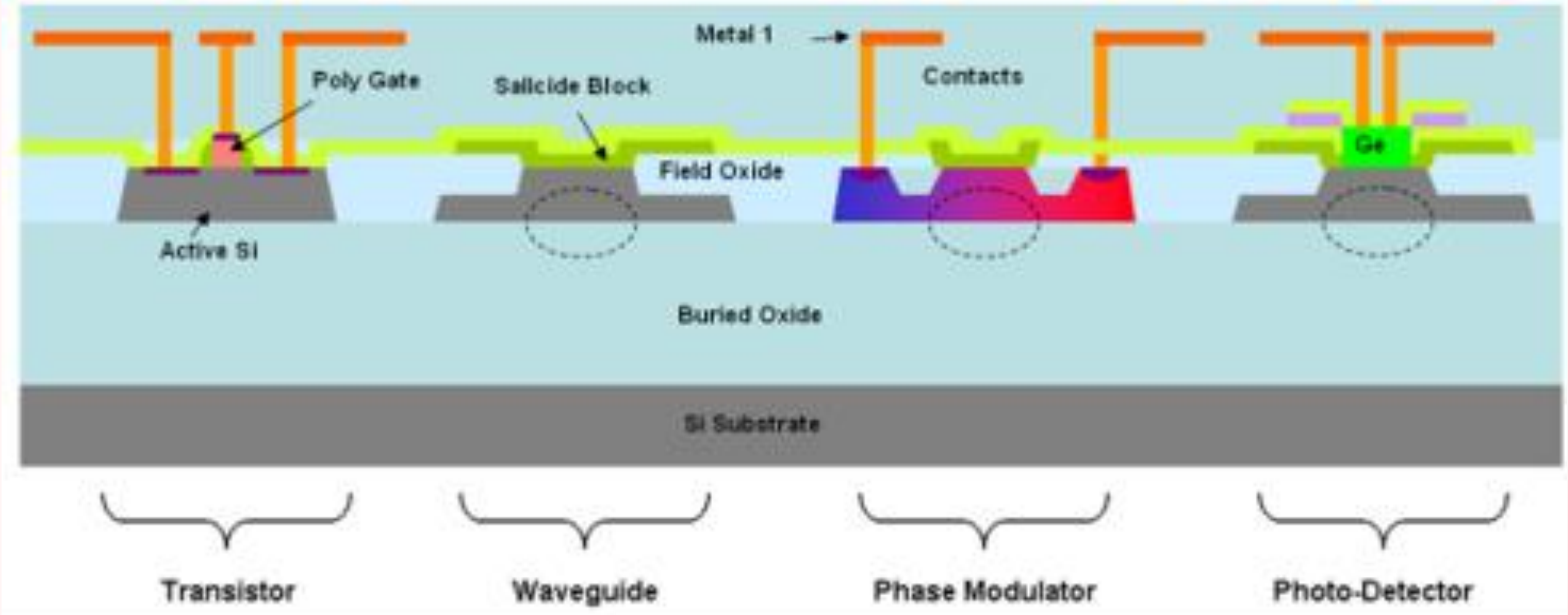
- Silicon photonics: low spectral dispersion, high refractive index

→ easy integration of complex optical system

→ chip-integrated communication systems for world-wide communication networks.

- SOI technology: Silicon optical components are built over a thick oxide layer previously deposited on top of a Si handling wafer.

Silicon On Insulator SOI



Quantum Computing

- 1982: R. P. Feynman proposed building a computer based on the manipulation of wavefunctions in order to simulate nature with quantum computer.
- 1994: P. W. Shor suggested an algorirthm to factorize integers into prime numbers operating on a quantum computer more efficent than the classical analogue.
- 2001: Knill, Laflamme and Milburn demonstrated how it is posible to use linear optics for quantum information processing using beam splitters, phase shifters, single photon sources and detectors.
- 2001-2002: T. C. Ralph, N. K. Langford, T. B. Bell and A. G. White proposed a NOT-controlled linear optical gate based on coincidence.

Controlled NOT (CNOT) gate

1 qubit: $\alpha_0|0\rangle + \alpha_1|1\rangle, \ |\alpha_0|^2 + |\alpha_1|^2 = 1$

Quantum logic gate for 1 qubit

$$X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix} \quad Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix} \quad R_\phi = \begin{pmatrix} 1 & 0 \\ 0 & e^{i\phi} \end{pmatrix} \quad H = \frac{1}{\sqrt{2}}\begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix}$$

2 qubits: $a|00\rangle + b|01\rangle + c|10\rangle + d|11\rangle$ $\quad |a|^2 + |b|^2 + |c|^2 + |d|^2 = 1$

Controlled NOT (CNOT) gate

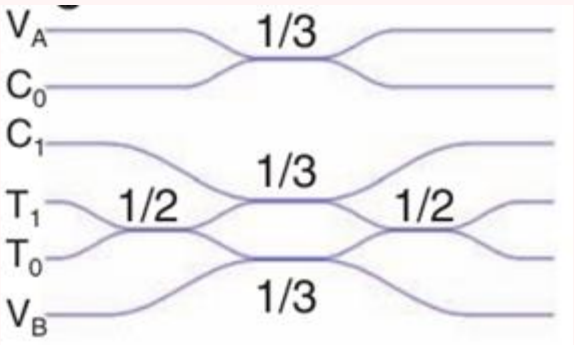
control bit

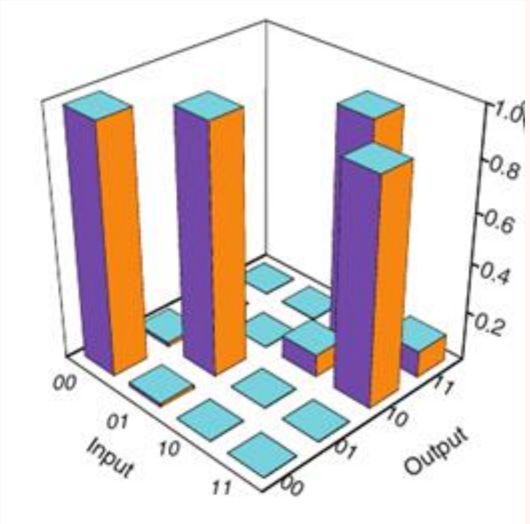
$$\mathrm{CNOT} = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix}$$

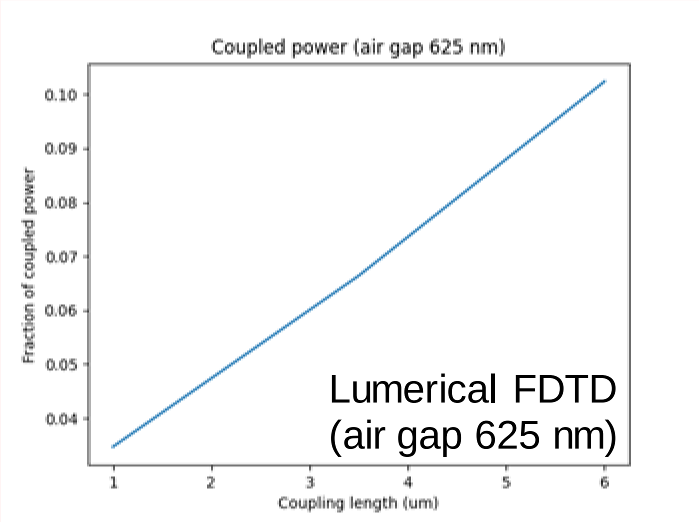
target bit

$$a|00\rangle + b|01\rangle + c|10\rangle + d|11\rangle \rightarrow a|00\rangle + b|01\rangle + c|11\rangle + d|10\rangle$$

CNOT-gate with Linear Optics in Silicon Photonic





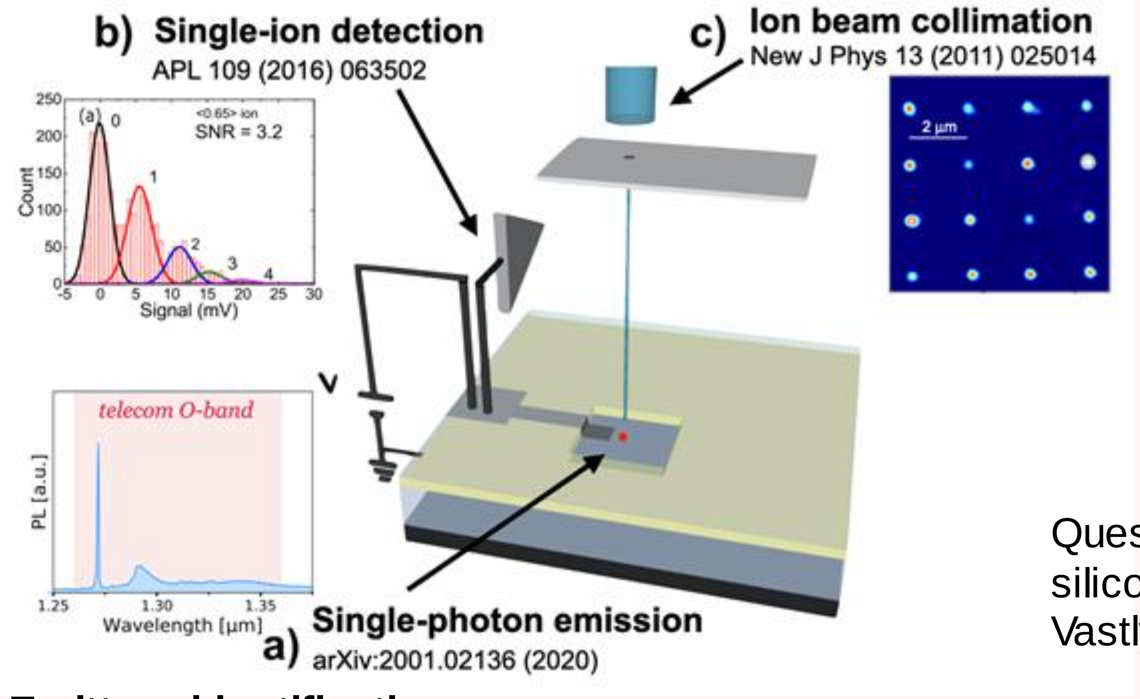


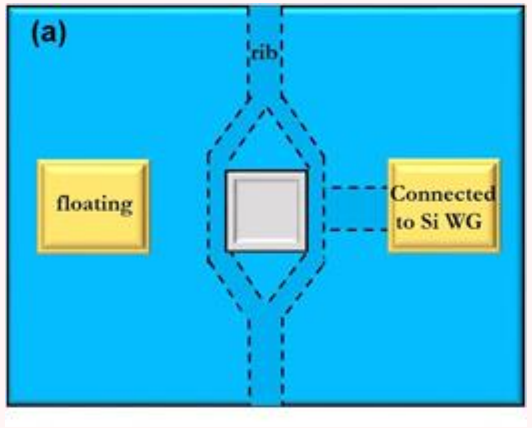
- Waveguide coupler used as beam splitter (η=1/2 e η=1/3)
- Coincidence basis (C_0T_0, C_1T_0, C_0T_1, C_1T_1)
- Postselected probabilistic gate (P=1/9)

T. C. Ralph et al, Linear optical controlled-NOT gate in the coincidence basis, DOI: 10.1103/PhysRevA.65.062324

A. Politi et al, Silica-on-Silicon Wavegide Quantum Circuits, DOI: 10.1126/science.1155441

Si-based single-photon sources at telecom wavelengths





Quest for single-photon sources based on defect in silicon at telecom wavelengths.
Vastly unexplored research field.

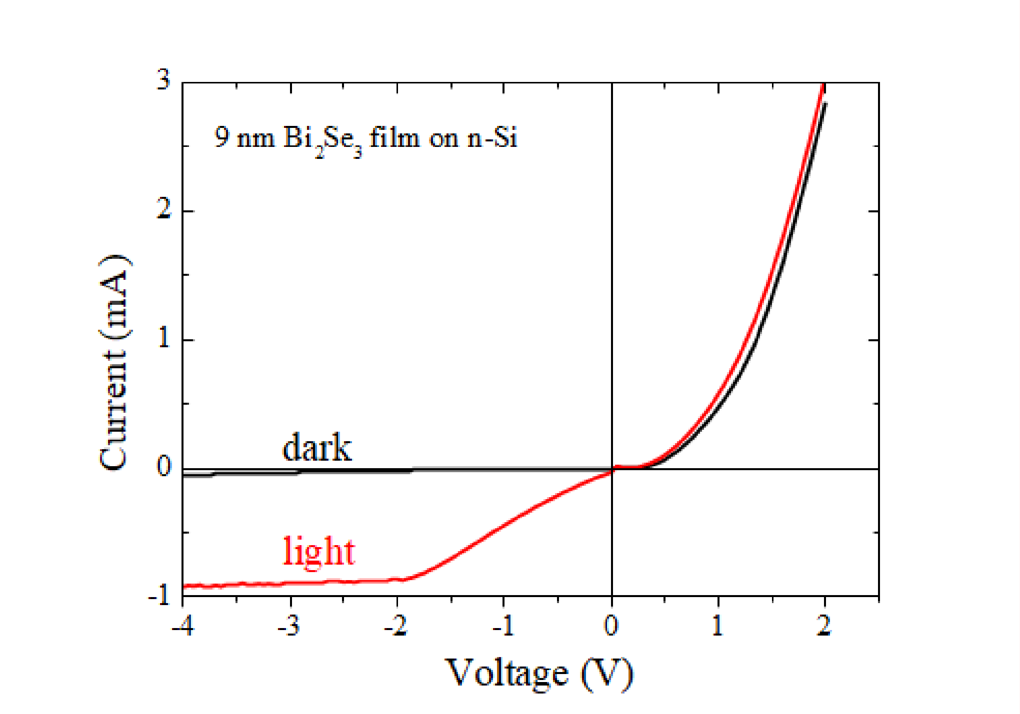
Emitters identification:

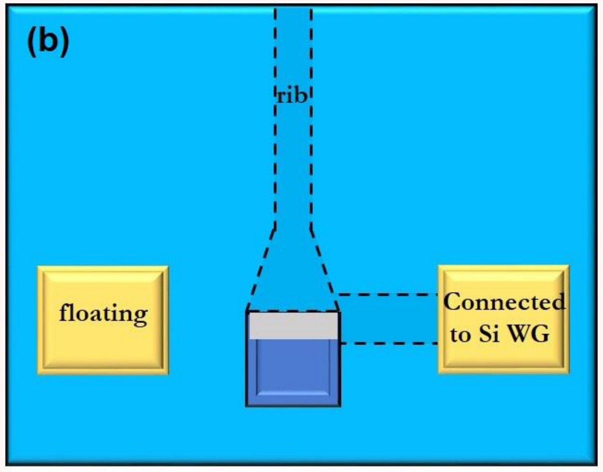
- screening of luminescent centers fabricated by ion implantation (group-IV, transition metals, halogens, He, …) at Leipzig Uni, Ruđer Bošković Inst, LNGS, LABEC
- exploitation of a custom irradiation chamber at the AN2000 LNL beamline
- development of a custom telecom confocal microscope
- identification and characterization of suitable single photon emitters

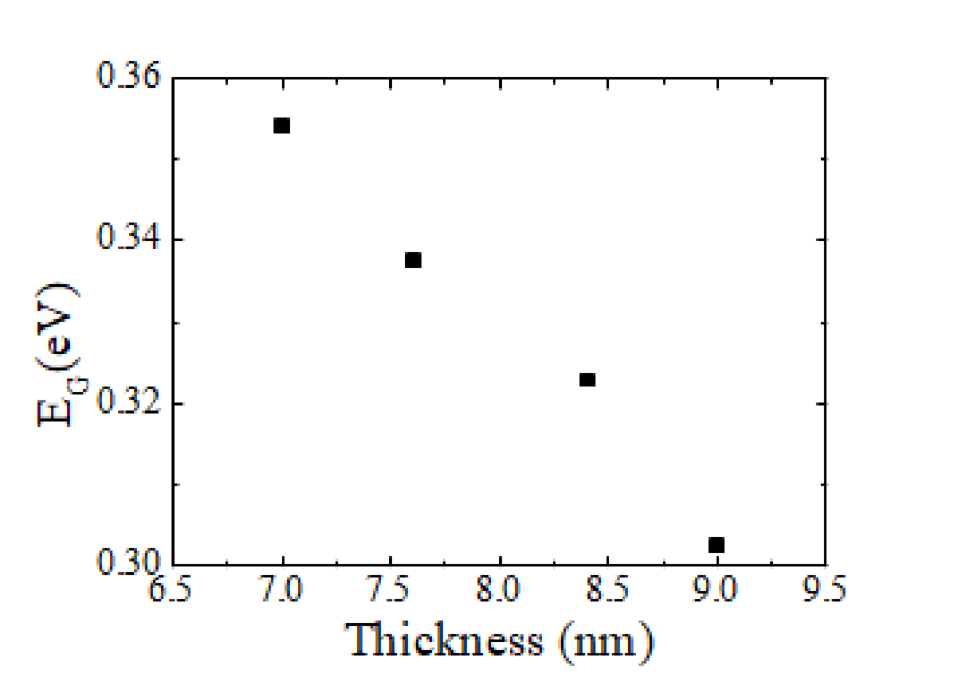
Emitters fabrication registered to the quantum circuit:

- ion implantation with sub-μm accuracy (collimation)
- single-ion delivery capability: the Si circuit is exploited as particle detector
- development of a custom irradiation chamber at the ion implanter

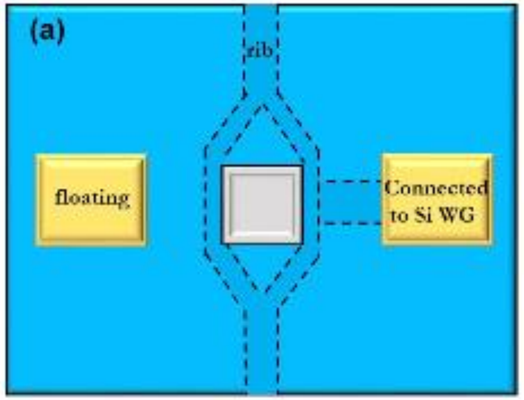
Single Photon Detectors (Bi_2Se_3/Si)



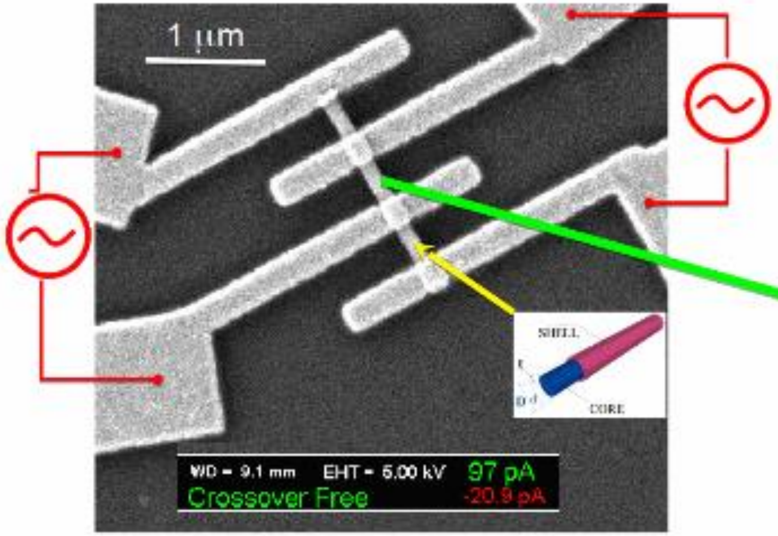




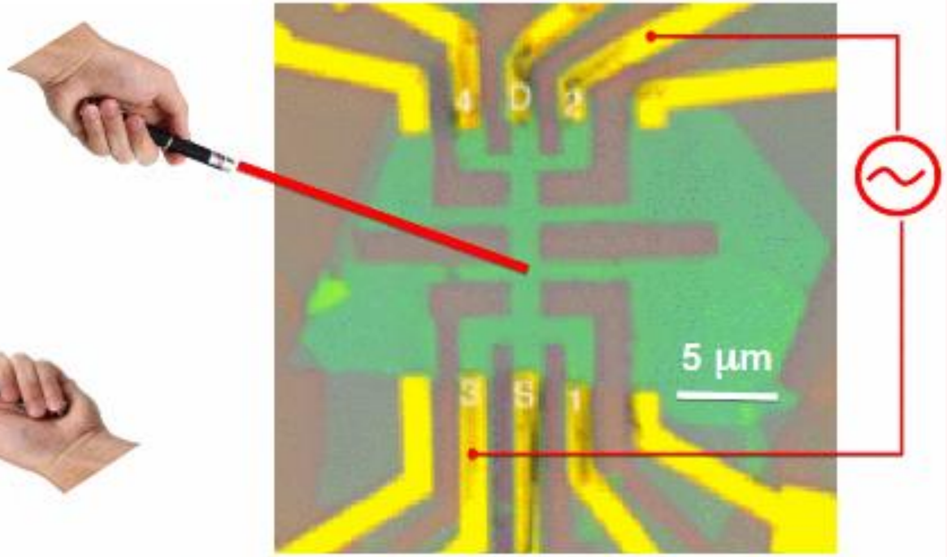
Polarization Control: 1D (nanowires) and 2D (Graphene, MoS2, …) materials on Si waveguides



A laser light and / or an external voltage can be used to control the quantum state of the electrons in the material and, due to proximity effects, the polarization state of the electromagnetic radiation in the wave guide.



InAs-GaSb nanowire (NW) with electrical connections, placed on Si.



Bilayer graphene encapsulates by hexagonal Boron Nitride with electrical connections, placed on Si.

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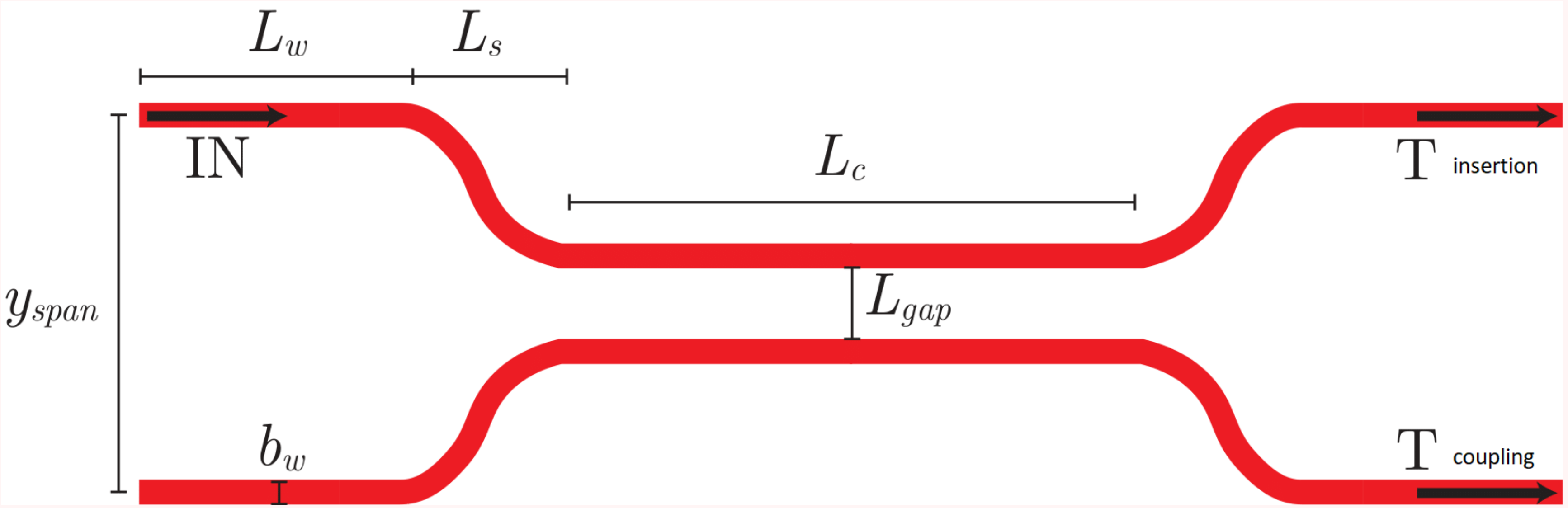
Directional coupler

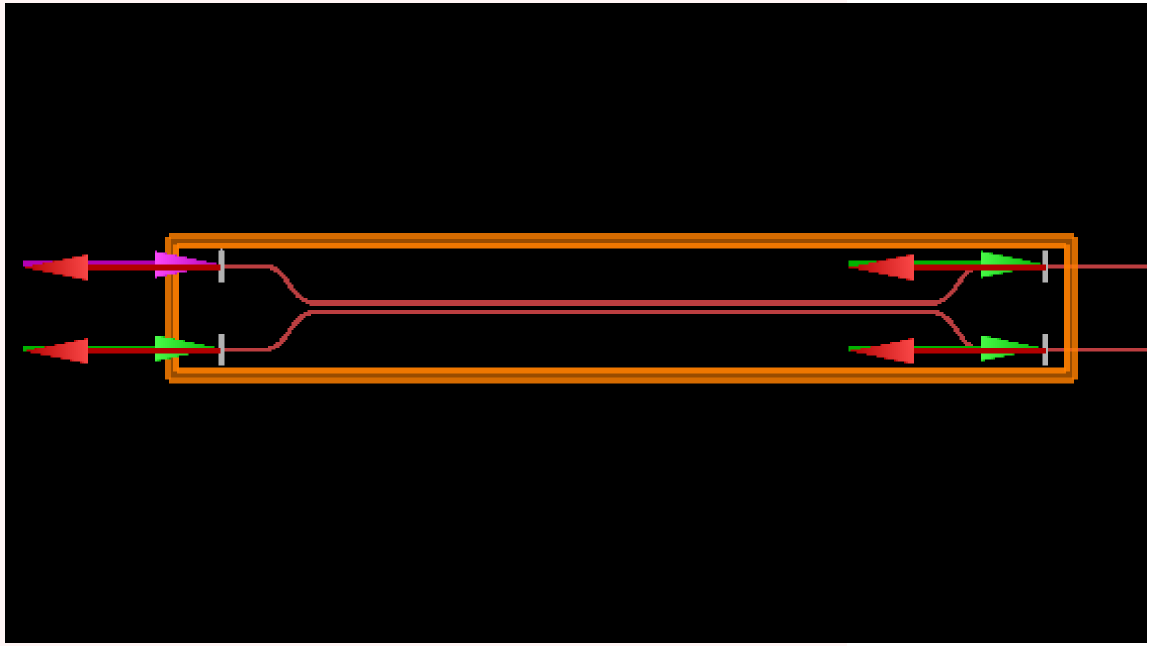
- FDTD simulation
- Properties of the directional coupler simulated:

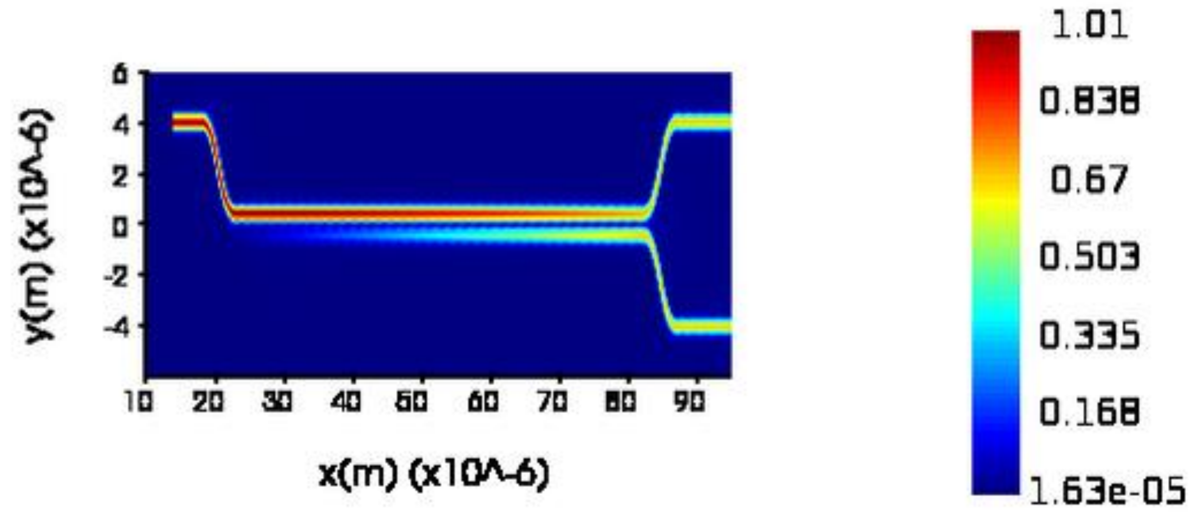
  Material: Silicon

  Width of the waveguide (b_w): 0.45 µm

  Height of the waveguide: 0.22 µm

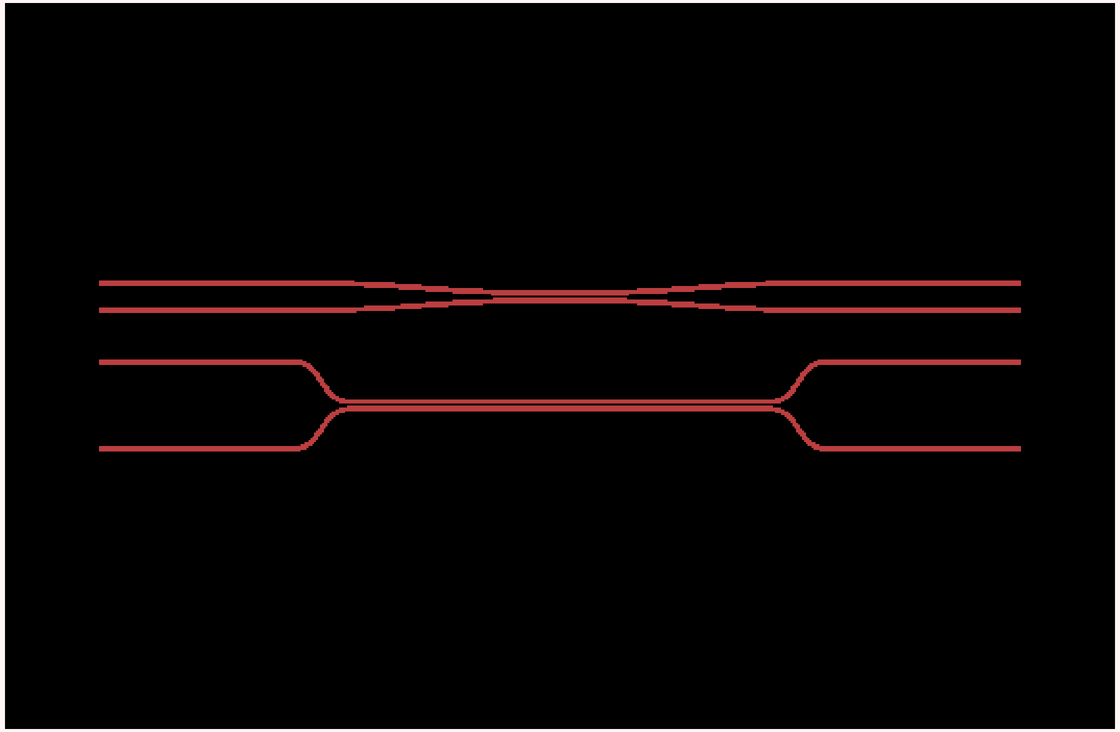


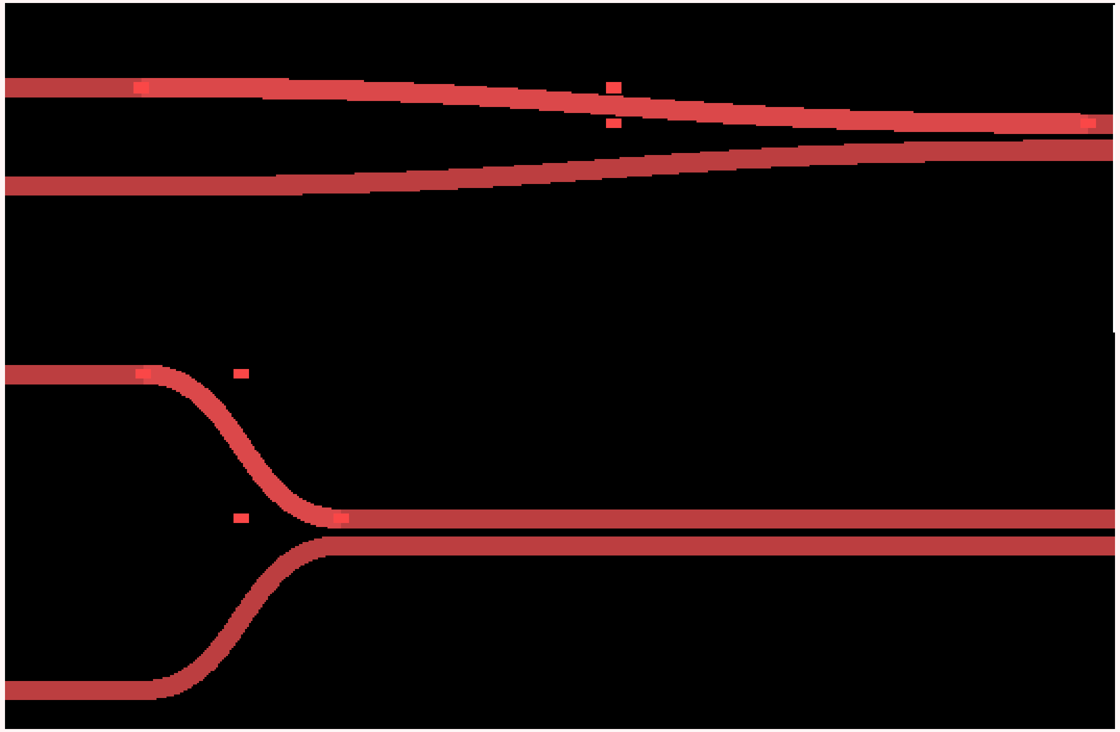




Top view (xy plane) of the directional coupler in the simulation box with 4 ports.

Electric field propagation at top view (xy plane).

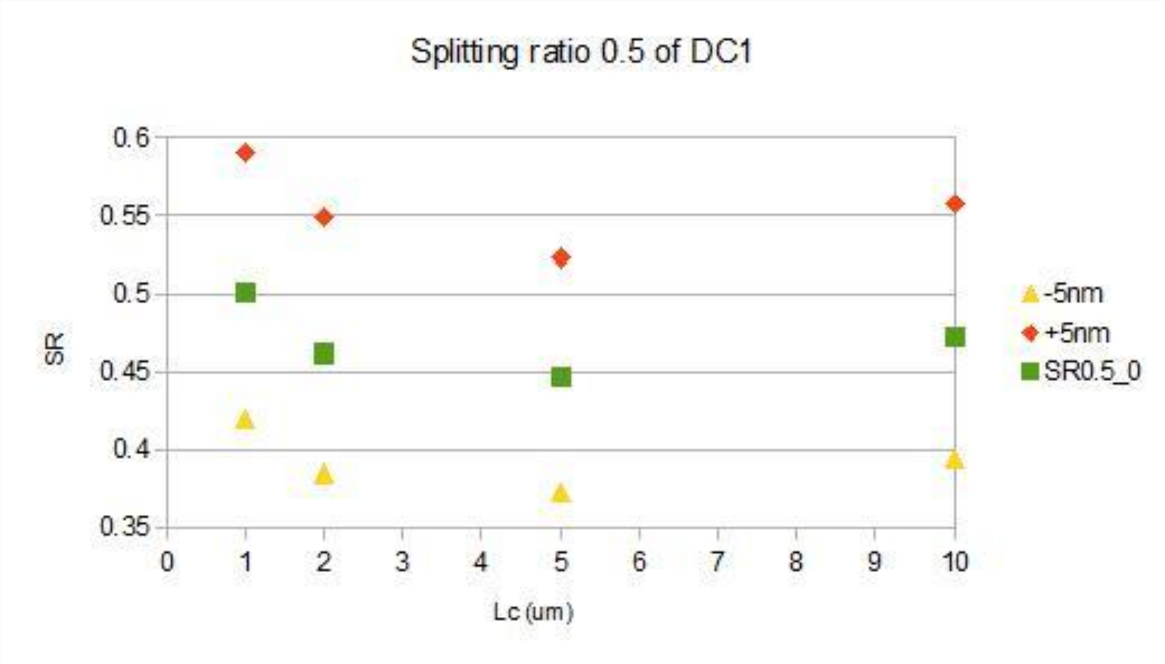


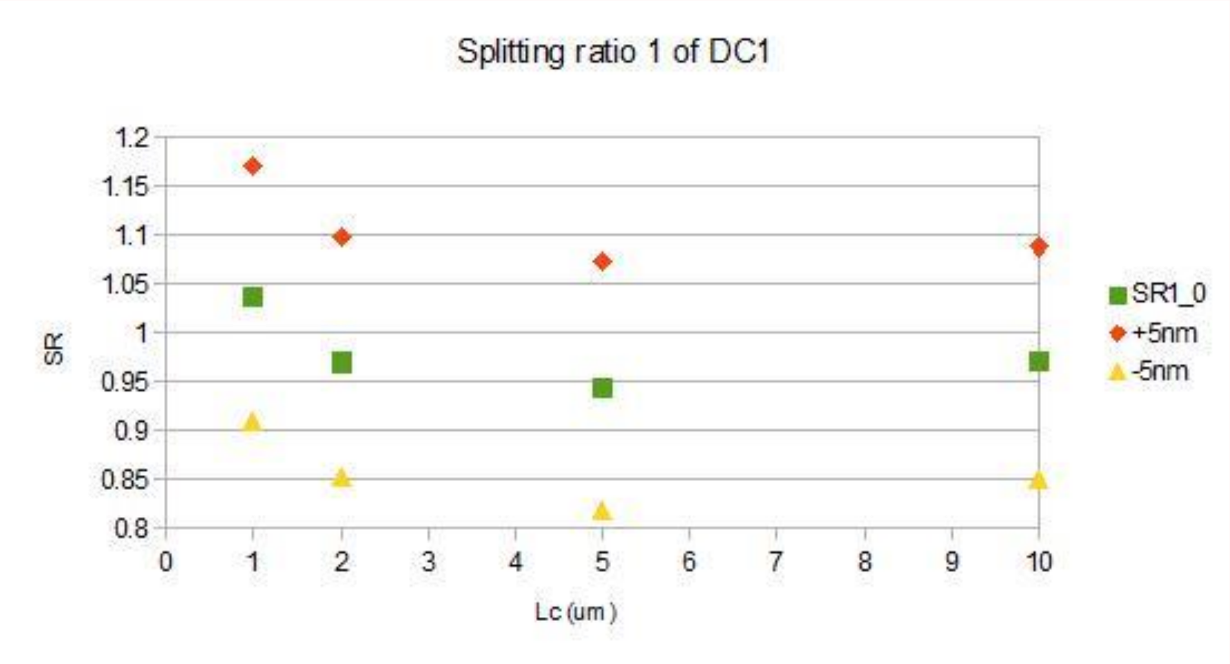


Top view (xy plane) of the directional couplers (DCs).

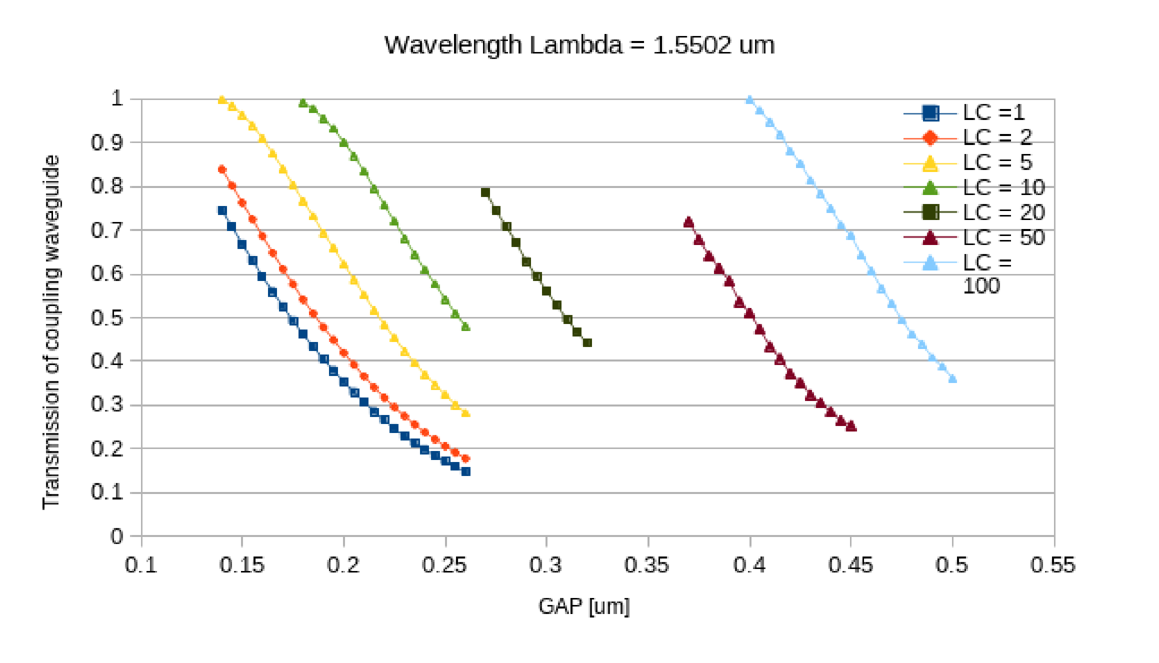
Bend top left parts of the 2 DCs

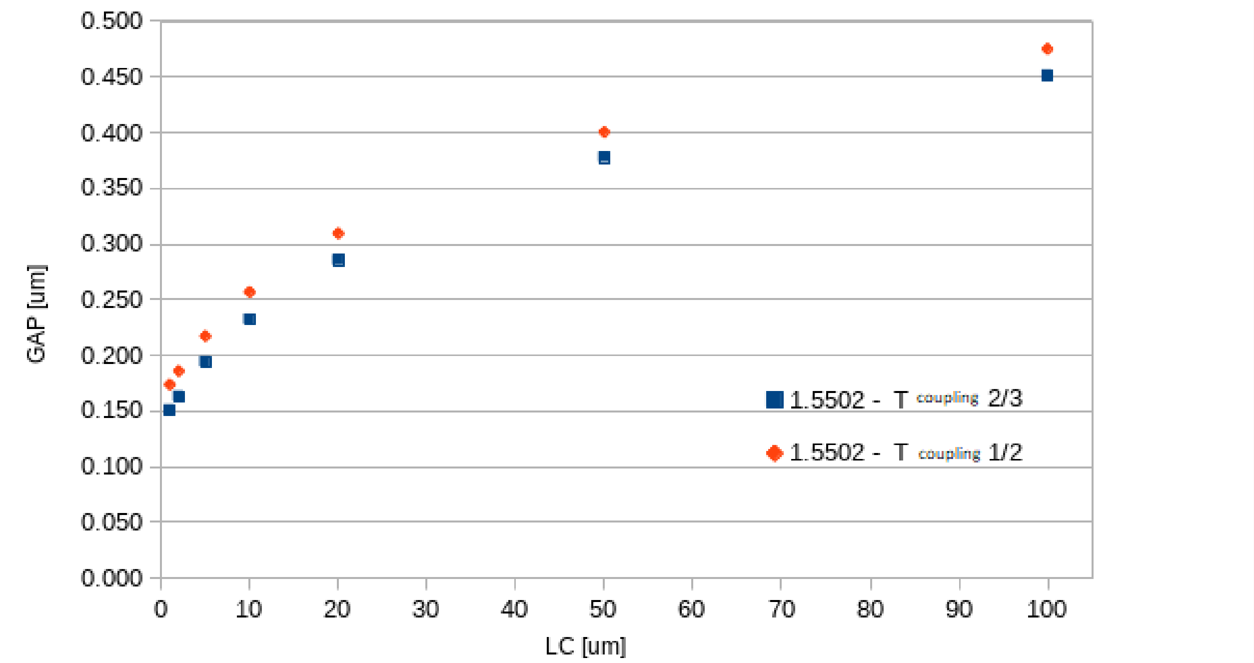
DC1 (upper): Lc1= 1μm, g=175nm, Ls1= 24μm, yspan1= 2.5μm;
DC2 (bottom): Lc2= 39μm, g=175nm, Ls2= 5μm, yspan2= 8μm.



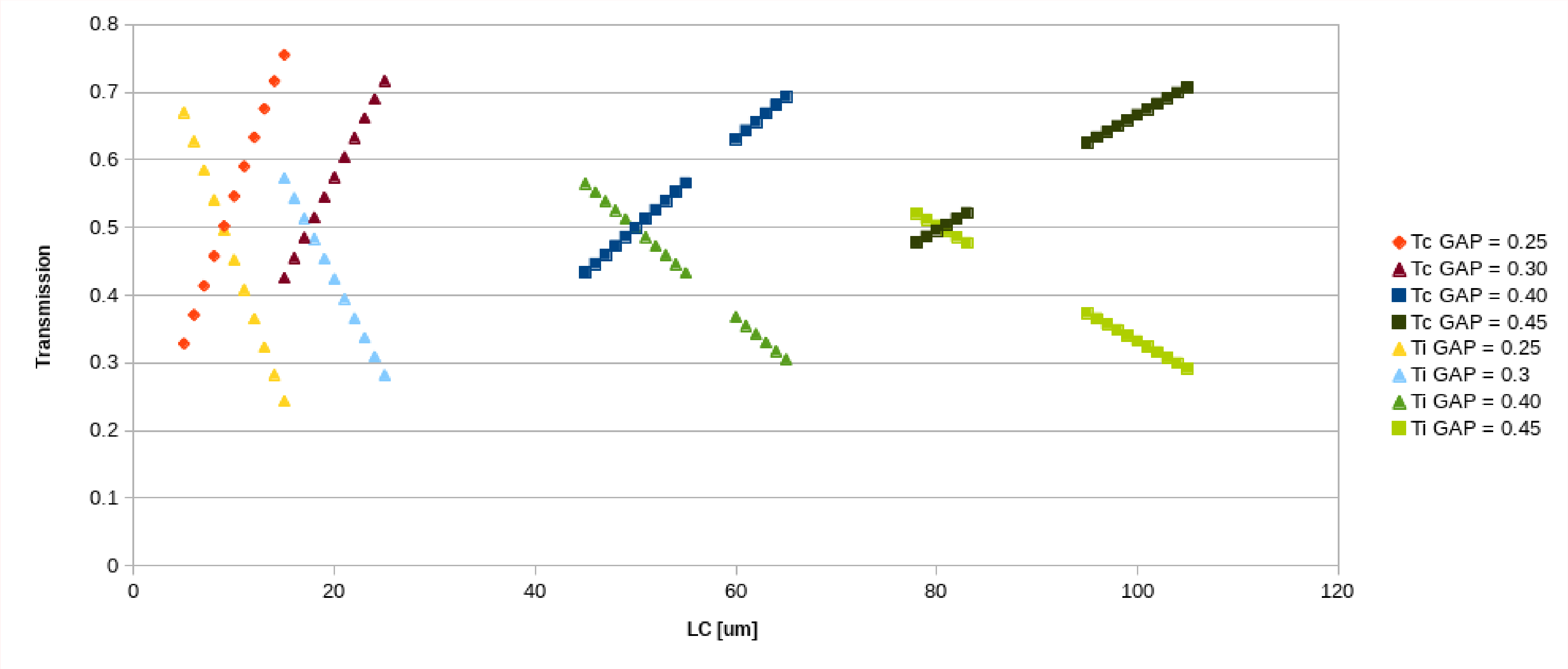


Splitting ratio (transmission output of insertion waveguide over coupling waveguide) SR=0.5 corresponding to 1/3-2/3 directional coupler, SR=1 corresponding to 1/2-1/2 directional coupler.

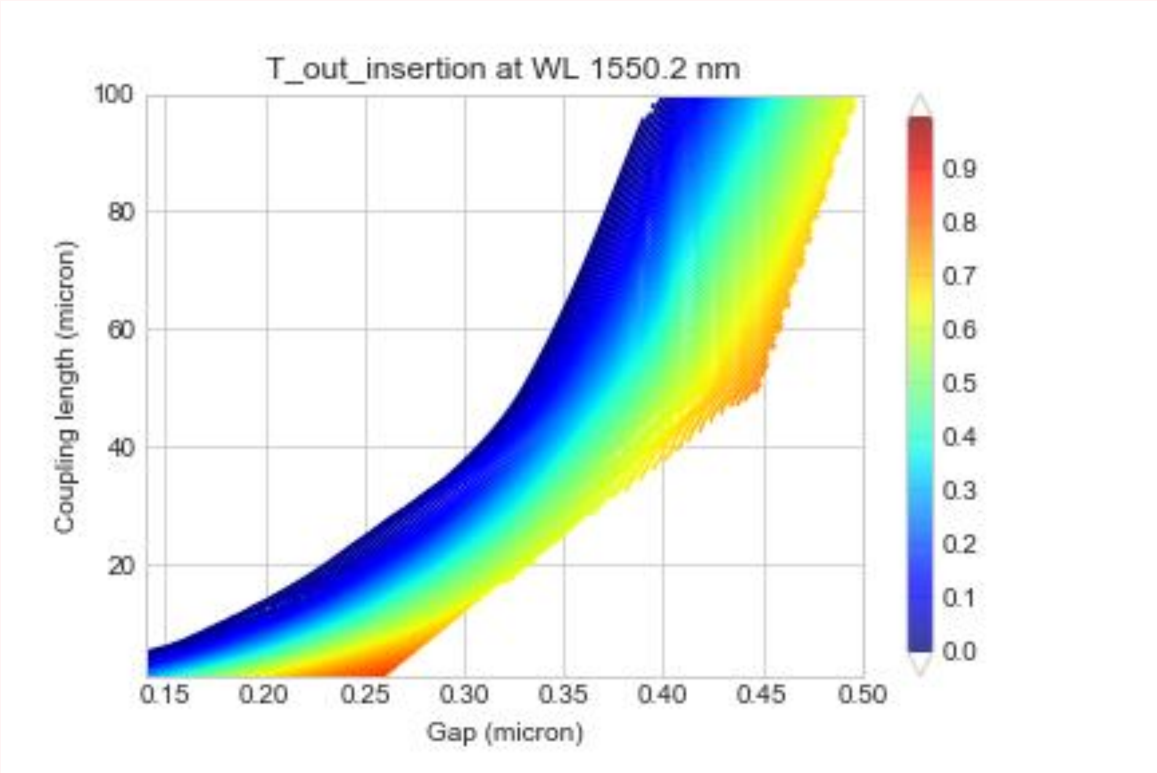


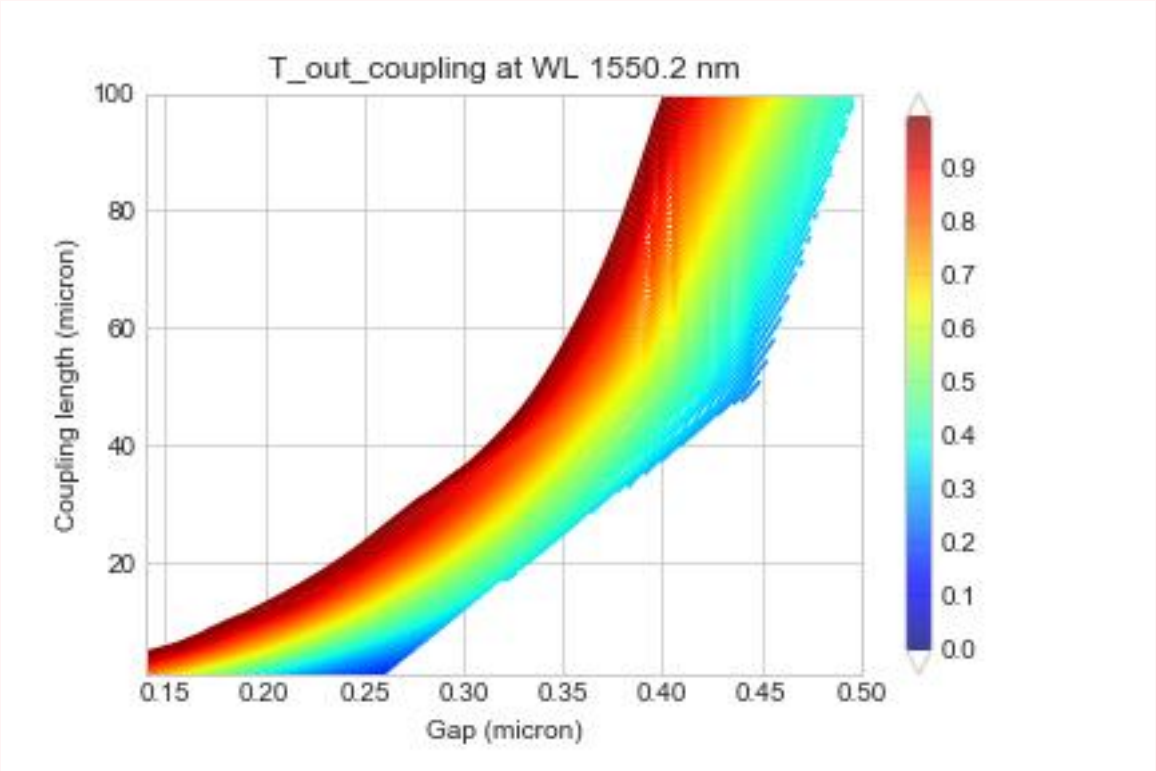


Ls= 24μm, yspan= 2.5μm

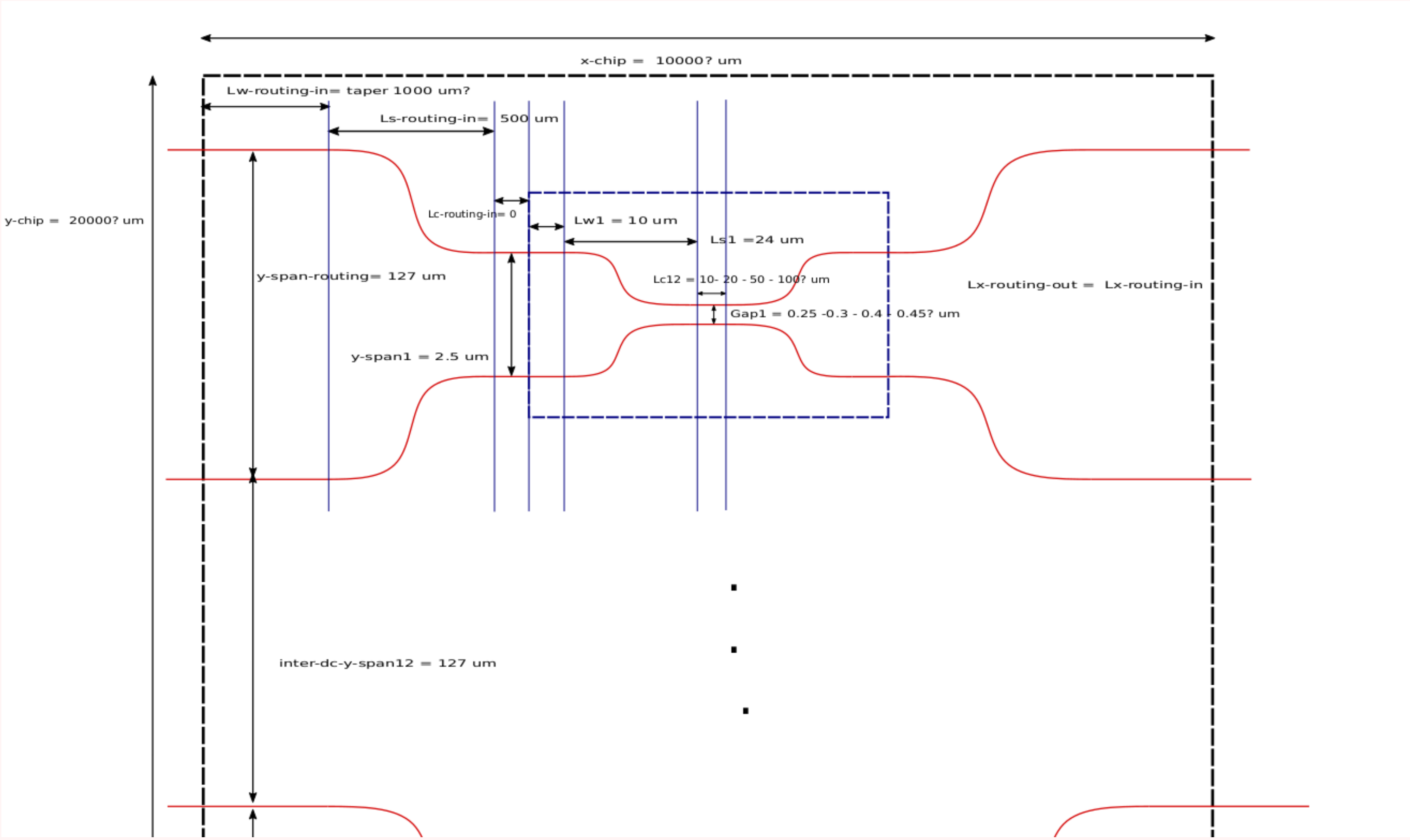


Ls= 24μm, yspan= 2.5μm





Ls= 24μm, yspan= 2.5μm



Design of the directional coupler on the chip. The input and output waveguides are spaced by 127μm such that they can be coupled with the standard V–groove fiber coupler produced by the company “PHIX B.V.”.

Thank you for your attention!